

ADC performance: time dependence

BNL DUNE

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Pre-introduction

This is an abbreviated version of DUNE DocDB 3633 v3

- [https://docs.dunescience.org:440/cgi-bin/RetrieveFile?
docid=3633&filename=adams_wip_20170608_adctimedep.pdf&version=3](https://docs.dunescience.org:440/cgi-bin/RetrieveFile?docid=3633&filename=adams_wip_20170608_adctimedep.pdf&version=3)
- See that note for all the missing plots
- And see later versions for updates

Introduction

I have been looking at ADC test data taken at BNL

- I report here on long-term data taken in March 2017
 - ADC samples are read out for input voltage steps with sawtooth envelope
 - 40M samples over 20s for each ADC channel
 - approximately 10k samples for each ADC bin
- Data is from new P1 chips for protoDUNE
- Data conditions
 - Cold (LN2)
 - There is warm data for one chip
 - 2 MHz sampling
 - All data taken with external clock
 - Single chip (D02) in board kept cold and powered
 - 18 samples taken over 10 days

Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

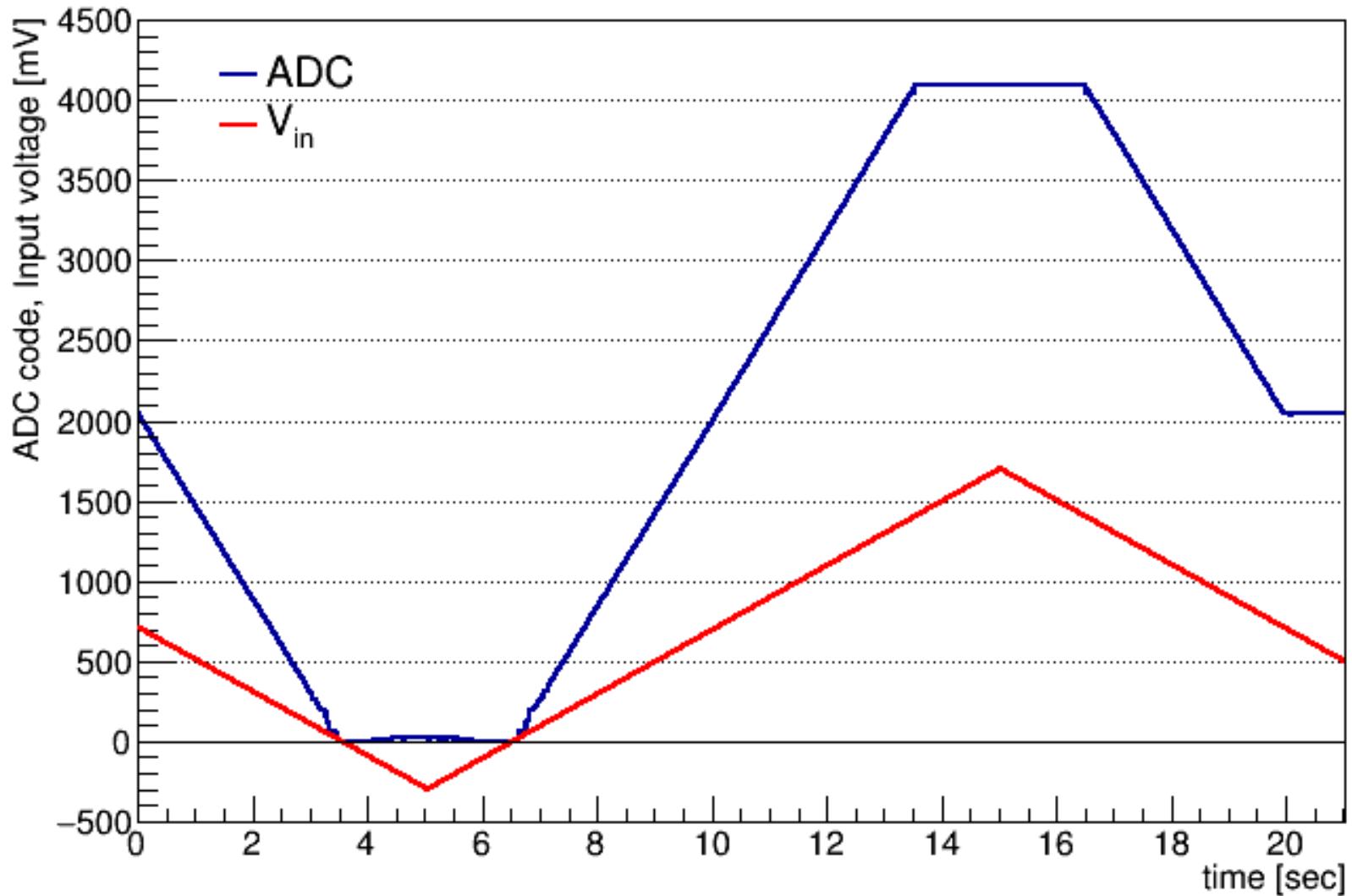
Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from –300 to 1700 mV at 200 mV/sec
- Data is approximately one period of sawtooth centered on the rise
 - See plot on following page
- I see ADC gets stuck at a value near 2000 after 20 sec
 - See following example plot
 - I keep only the first 19.8 sec of data for each sample
 - Waveform plots show all samples then look OK

Example waveform

201703b_D02_6b channel 4



Data analysis

Data is analyzed as described in previous talks

- Also see appendix

First need input voltage

- This was provided by data takers for earlier samples
 - Those were in CSV format with one rise starting at a specified voltage
- Here data is ADC only (channel number packed in high bits)
 - Known waveform: sawtooth with 10 s rise/fall over (-300, 1700) mV
 - But time offset is not specified
- I determine the min and max points from ADC data in two ways
 - Data above or below a double threshold
 - Midpoints between peaks in the ADC bin distributions
 - Require these to agree with one another
- Assume the min and max found in this way correspond to the same for the input voltage → timing offset and period
- Preceding plot shows V_{in} determined in this way

Results

Performance plots are in appendix

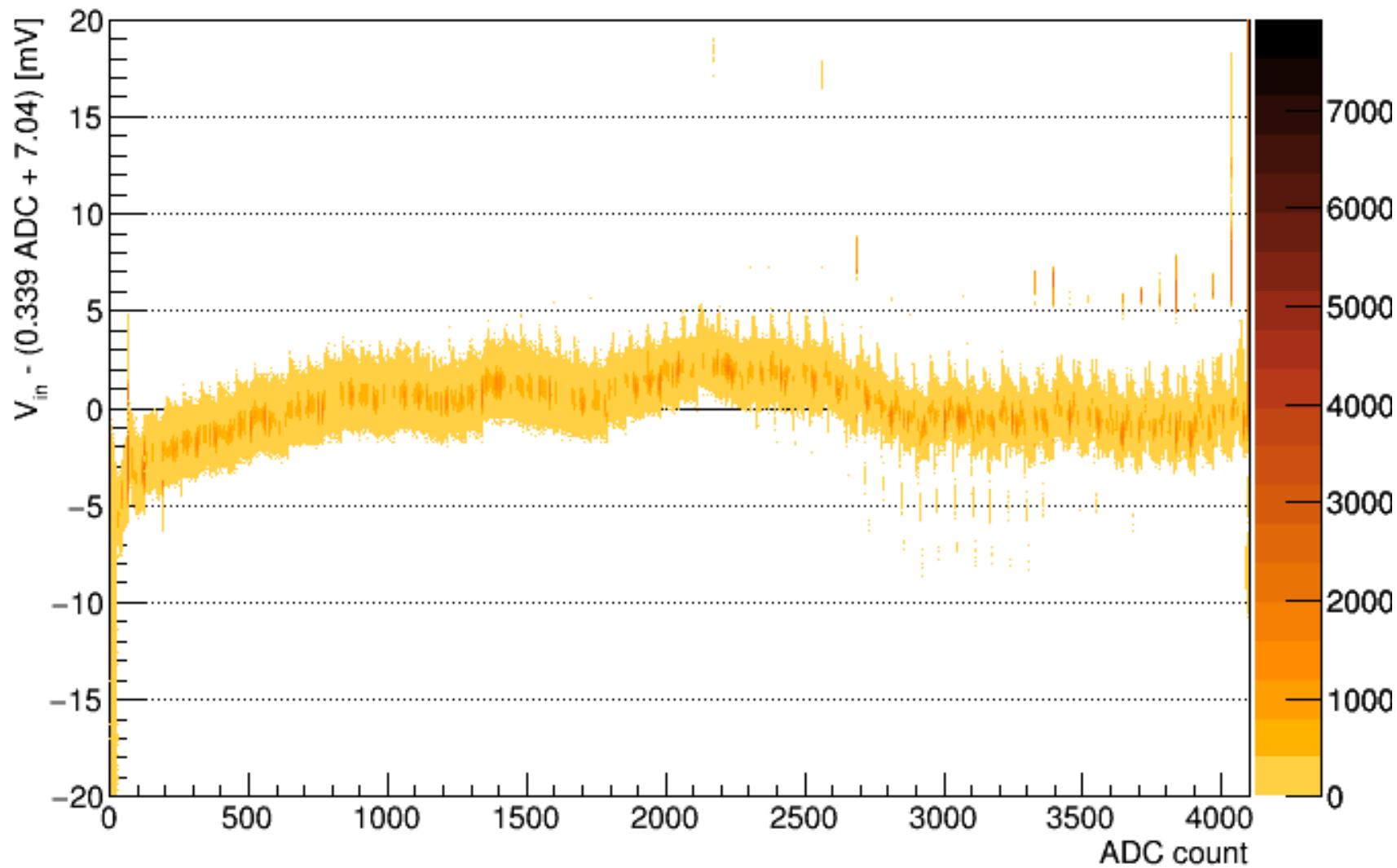
- 18 samples for one chip
- Taken over 10 days

Comments

- Bulk response seems very consistent day-to-day
 - Overall gain RMS is 3.6% (primarily channel-to-channel variation)
 - Largest gain RMS for any one channel is 0.03%
 - No bulk changes evident in residual spectra
- There is some change in the bad channels and tails
 - Many the same day after day but some appear or disappear
 - Biggest changes in channel 6—a few plots for it on the following pages
 - Many plots for all channels and times in appendix 2
- Work in progress to quantify these changes
 - E.g. what are bad and tail fractions if we combine all samples or take the worst of each?
 - Effect of using the “wrong” sample to identify problems

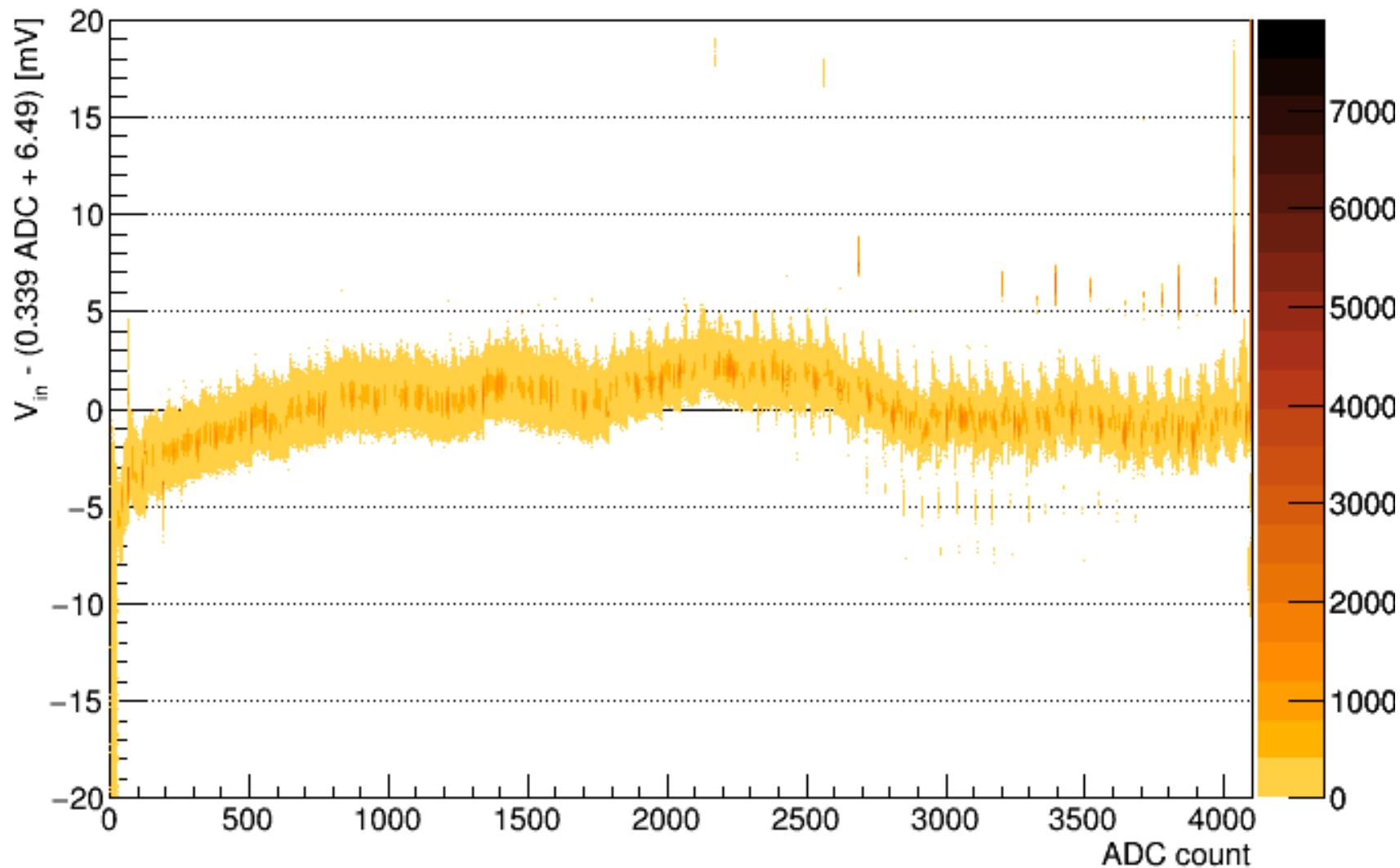
Chip D02, time 1a

201703b_D02_1a channel 6



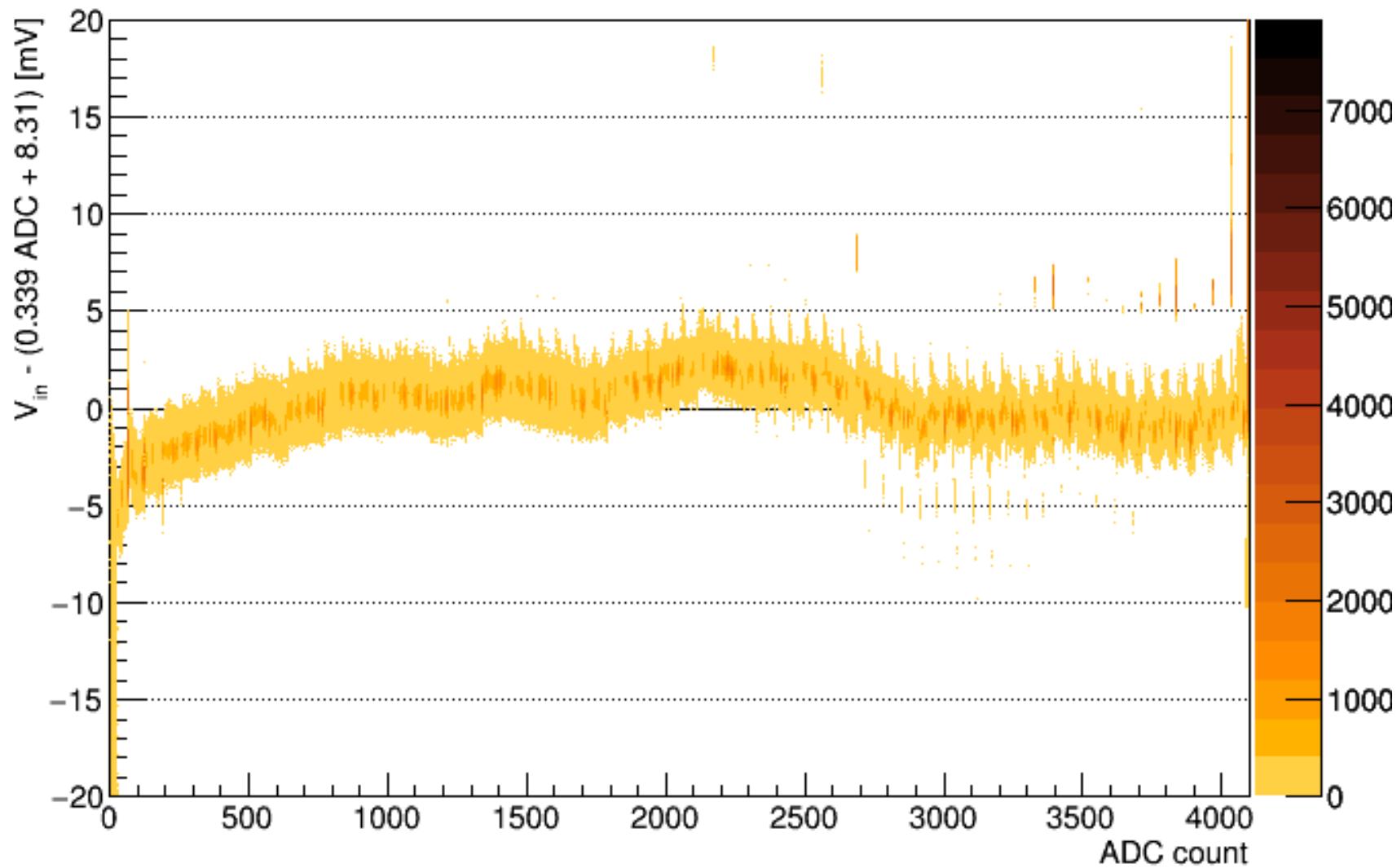
Chip D02, time 2a

201703b_D02_2a channel 6



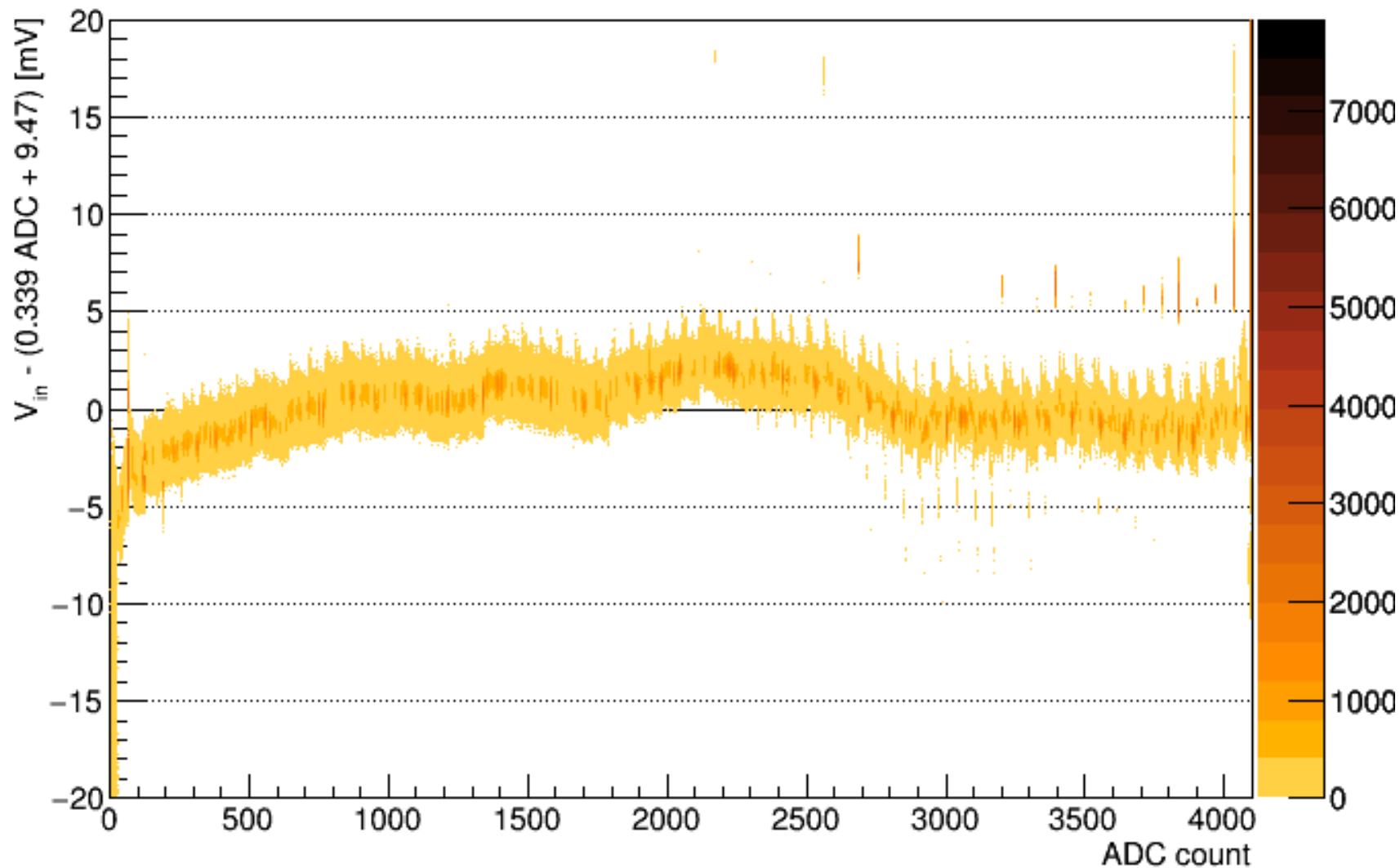
Chip D02, time 3a

201703b_D02_3a channel 6



Chip D02, time 3b

201703b_D02_3b channel 6



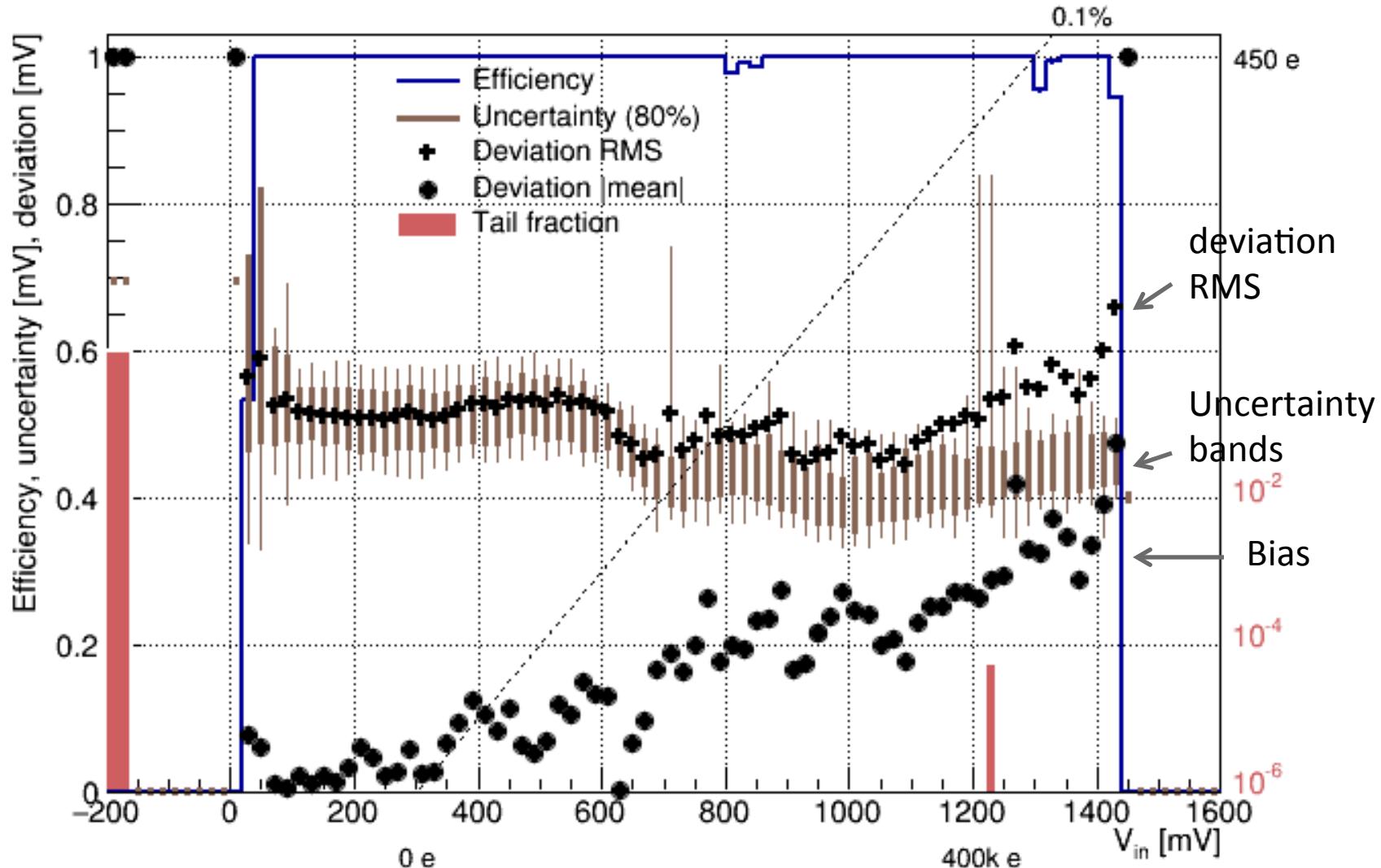
Calibrated performance: Introduction

I studied the effect of using calibration from a different time

- Calibration generated from the first time sample
 - Usual ultimate calibration with separate constant for each ADC bin
 - Bins with low counts or RMS > 1.0 mV are skipped (inefficiency)
- Look at performance for each of the 18 time samples using that calibration
 - Compare V_{meas} , the voltage obtained by applying the calibration to the recorded ADC bin, with V_{true} , the voltage from the sawtooth waveform
 - A pedestal is added to the calibration so that it gives the same average response over a small ADC range near 300 mV
 - Simulate the effect of removing voltage offsets with pedestal data
 - Without this, there are big differences between time samples
 - » Change in the pulser offset or a change in the chip?
 - Add two variable to the performance plots
 - Bias: mean deviation ($V_{\text{meas}} - V_{\text{true}}$) (absolute value is plotted)
 - RMS($V_{\text{meas}} - V_{\text{true}}$)—includes response changes between the two samples and the resolution of the tested sample

Calibrated performance: Example plot

201703b_D02_4a channel 10 actual performance for RMS < 1 mV, calib 201703b_0606_chip2_chan10_time1488819180_ped



Calibrated performance: Results

Results

- If the calibration were perfect, we expect the bias to be (close to) zero and the RMS deviation to appear with the uncertainty error bands
 - The first sample (calibrated with itself) shows this behavior
- The remaining samples show some degradation
 - Example plot on preceding page
 - Full set of plots (“Calibrated performance”) in the appendix
 - One of these on the following page
- The degradation is small: less than 0.1% except for very small signals where it is still less than 100 e (for gain 14 mV/fC)
 - And much of the degradation is due to a linear gain variation that may be due to pulser variations or could easily be corrected with calibration data
- Performance plots also show tails
 - Just a little bit worse with the “wrong” calibration
 - May want to use multiple time samples to find bins with tails and then flag these as bad → smaller tails but lower efficiency

Comments/Conclusions

ADC does show some time dependence

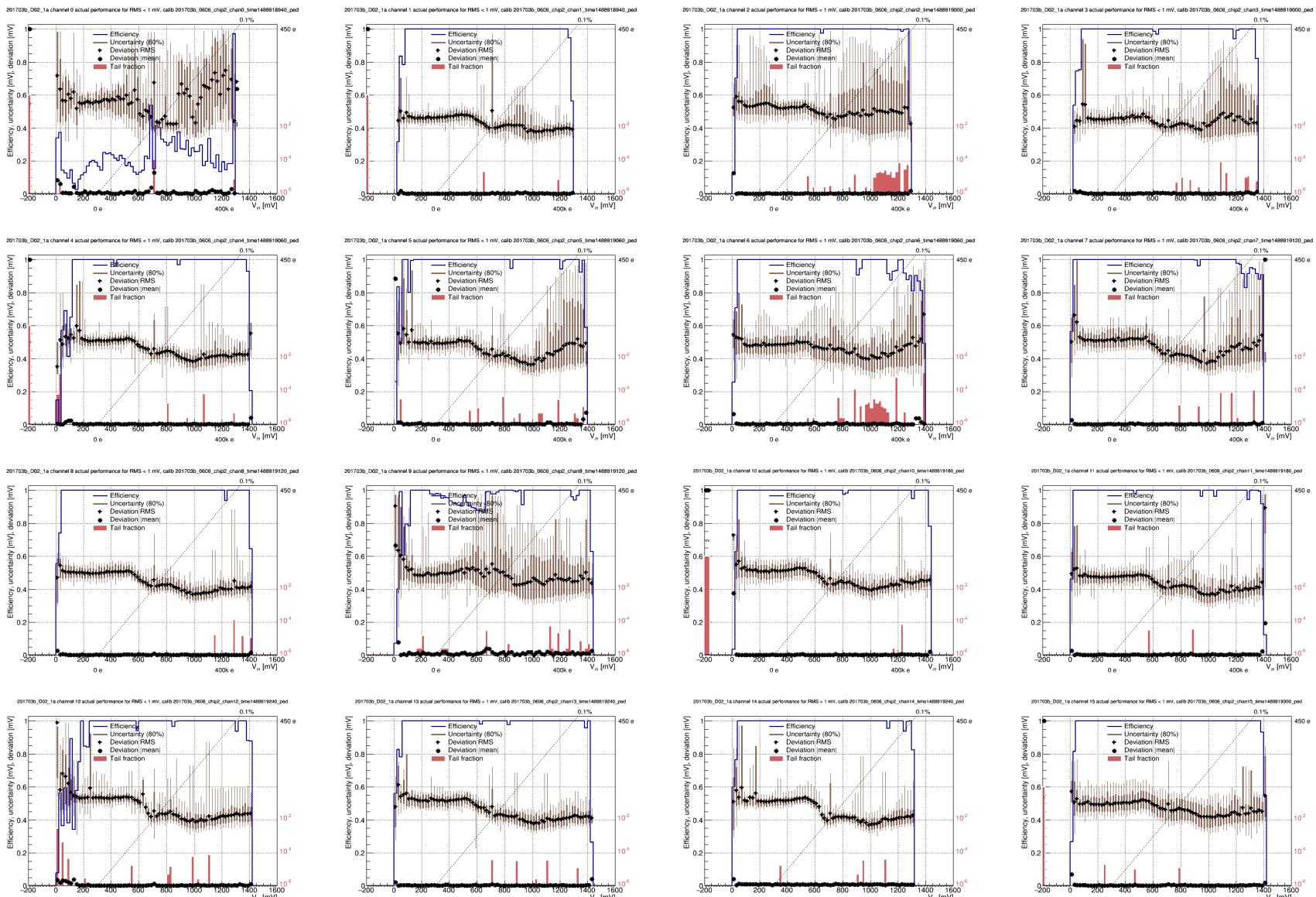
- For chip in board, kept cold and powered
- Gain is very stable
- Residual from linear calibration is also pretty stable
- But there are changes in bad channels (RMS) and tails day-to-day
 - About 0.2% of bins show “significant variation”
 - Probably want to look at multiple ramps to identify all bad/tail channels
- Calibration holds up well for 10 days (< 0.1% degradation)

Next

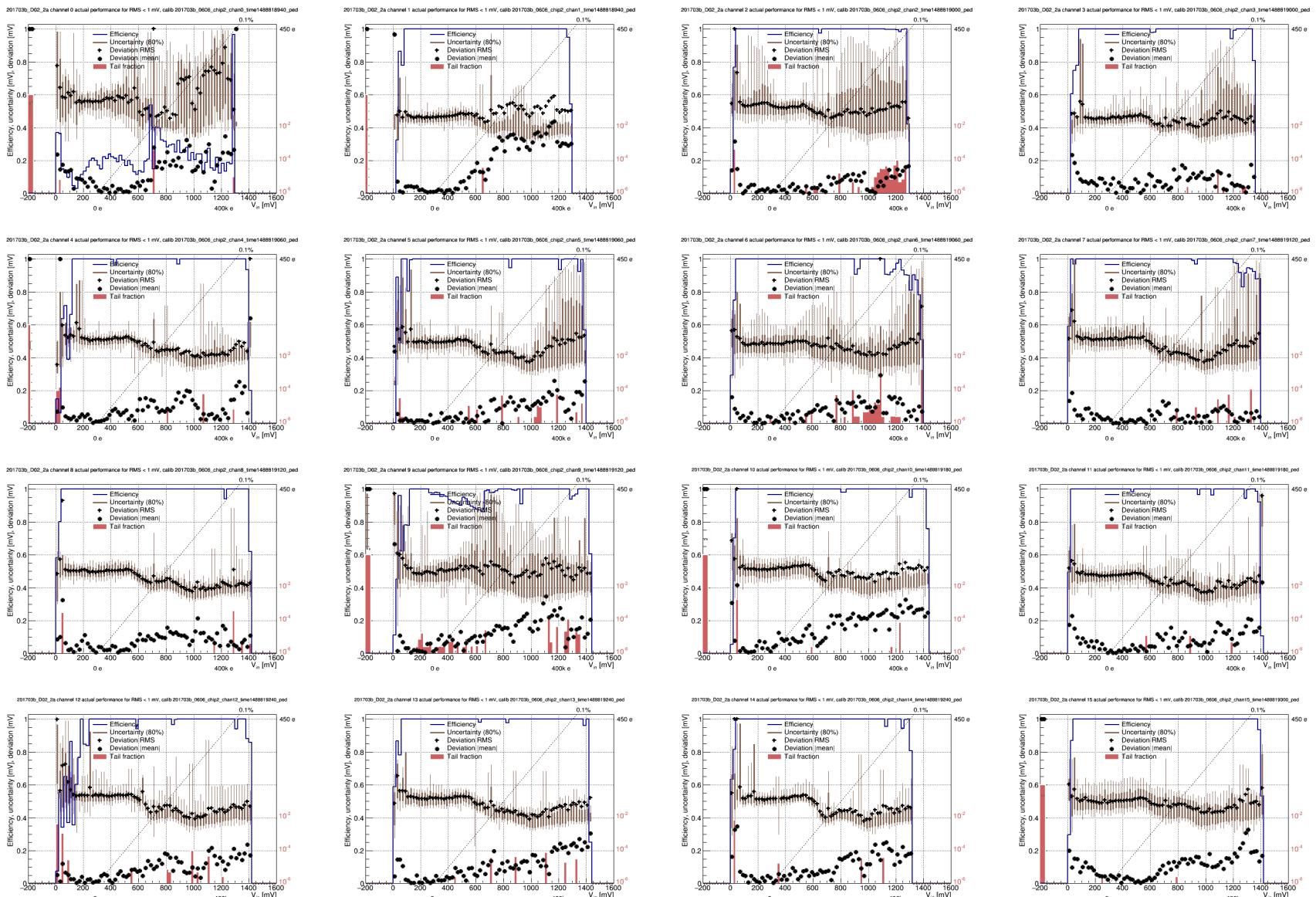
- Performance summary plot where bins are declared bad if they appear bad in any of the time samples

Calibrated performance

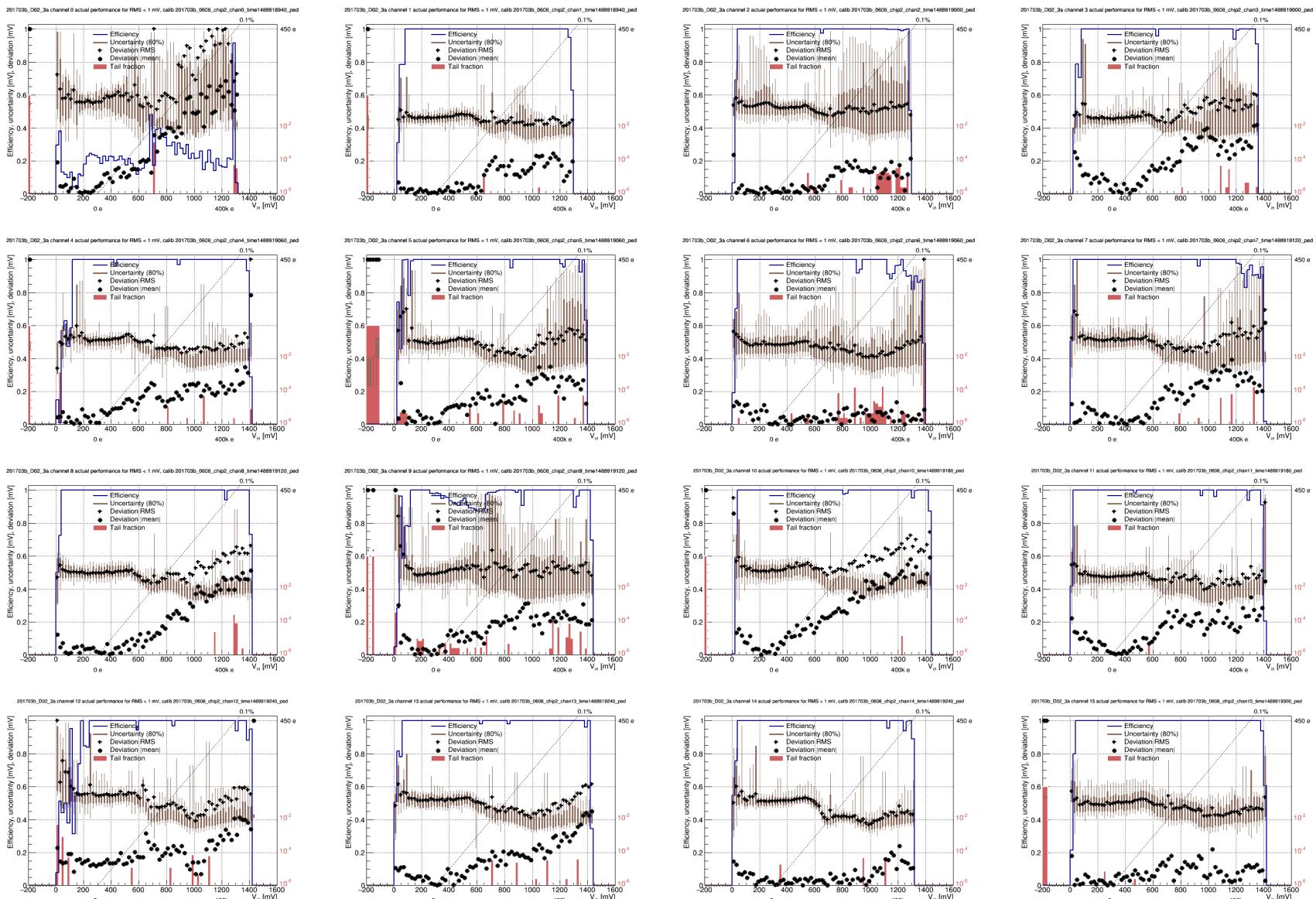
Calibrated performance: chip D02, time 1a



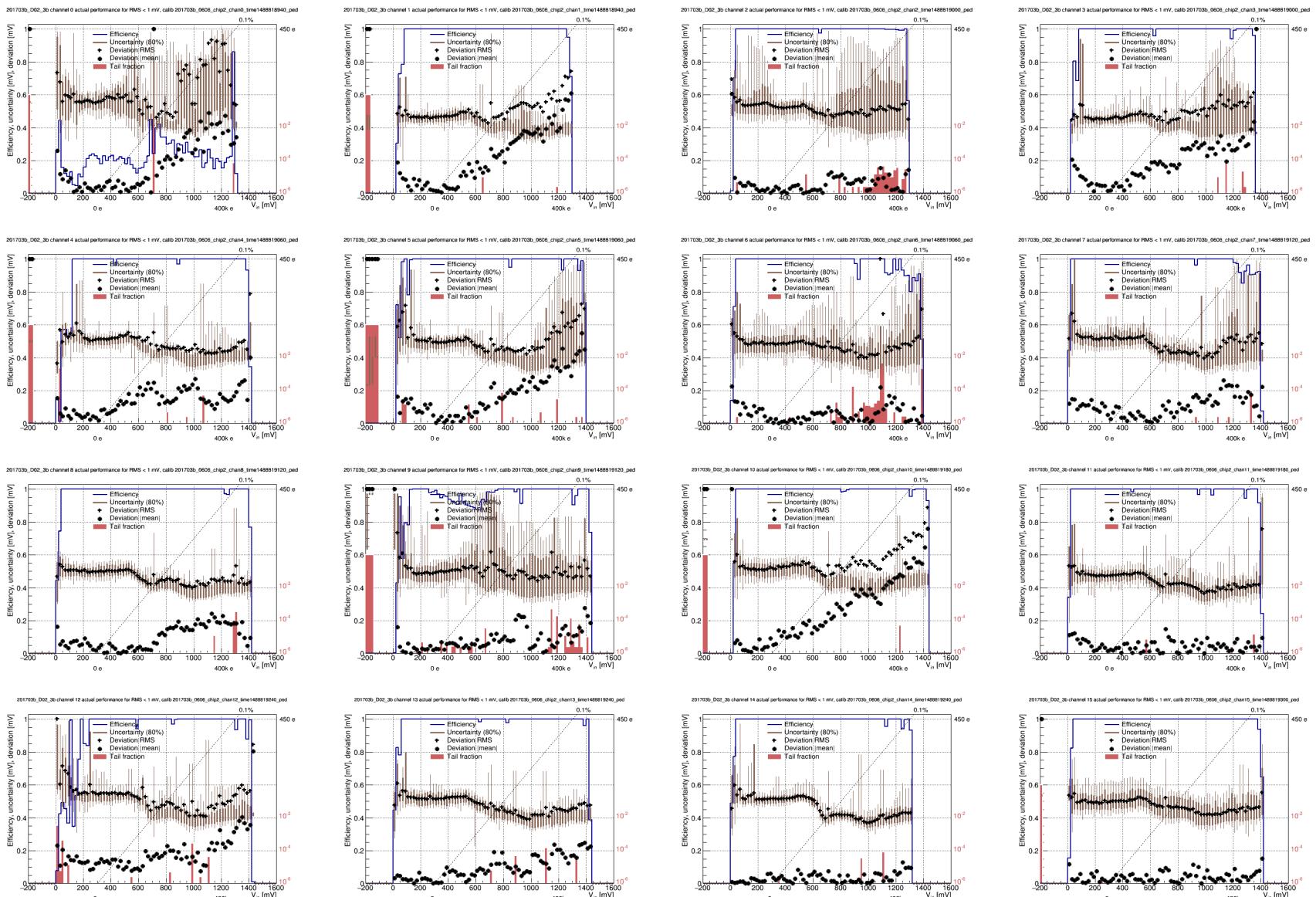
Calibrated performance: chip D02, time 2a



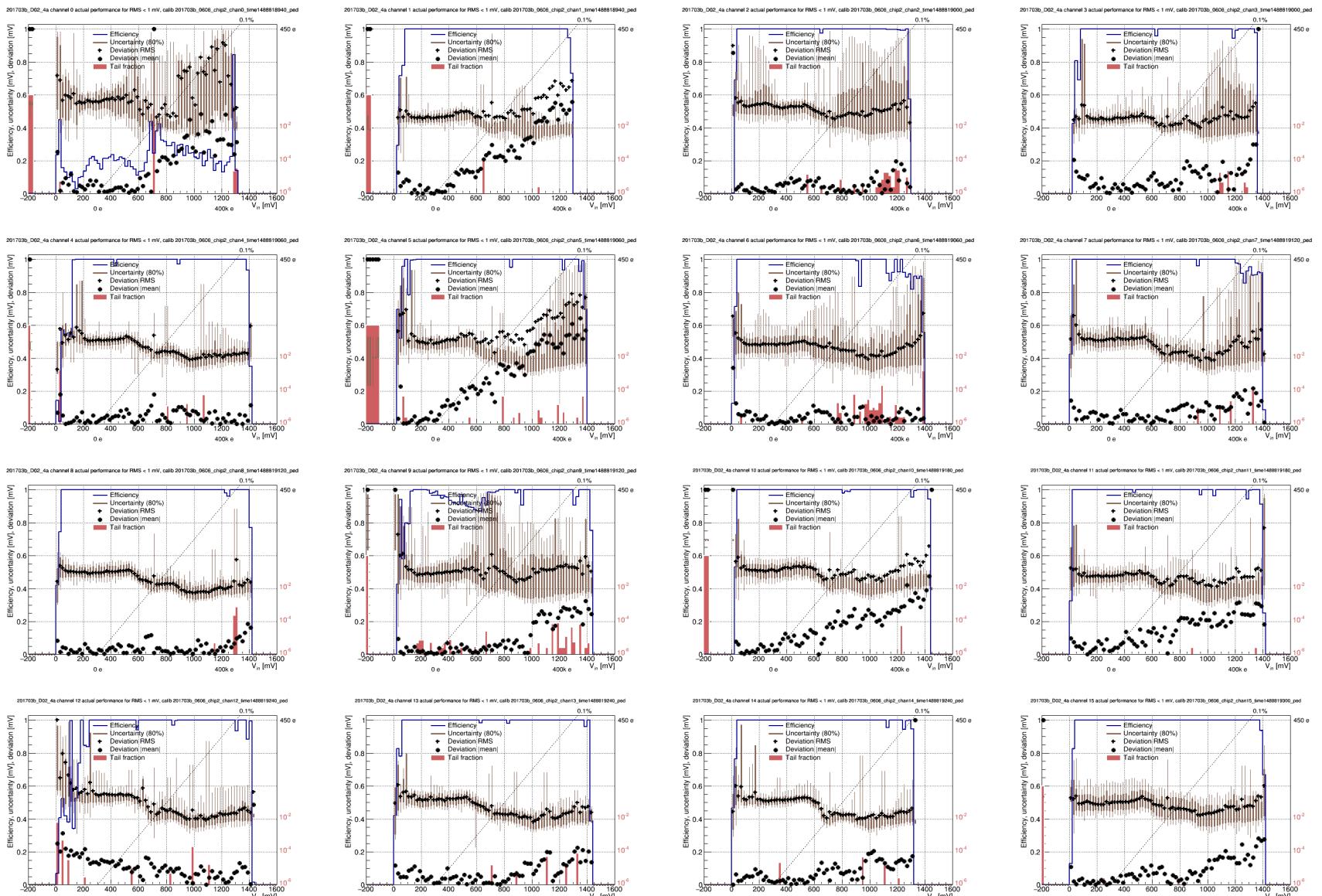
Calibrated performance: chip D02, time 3a



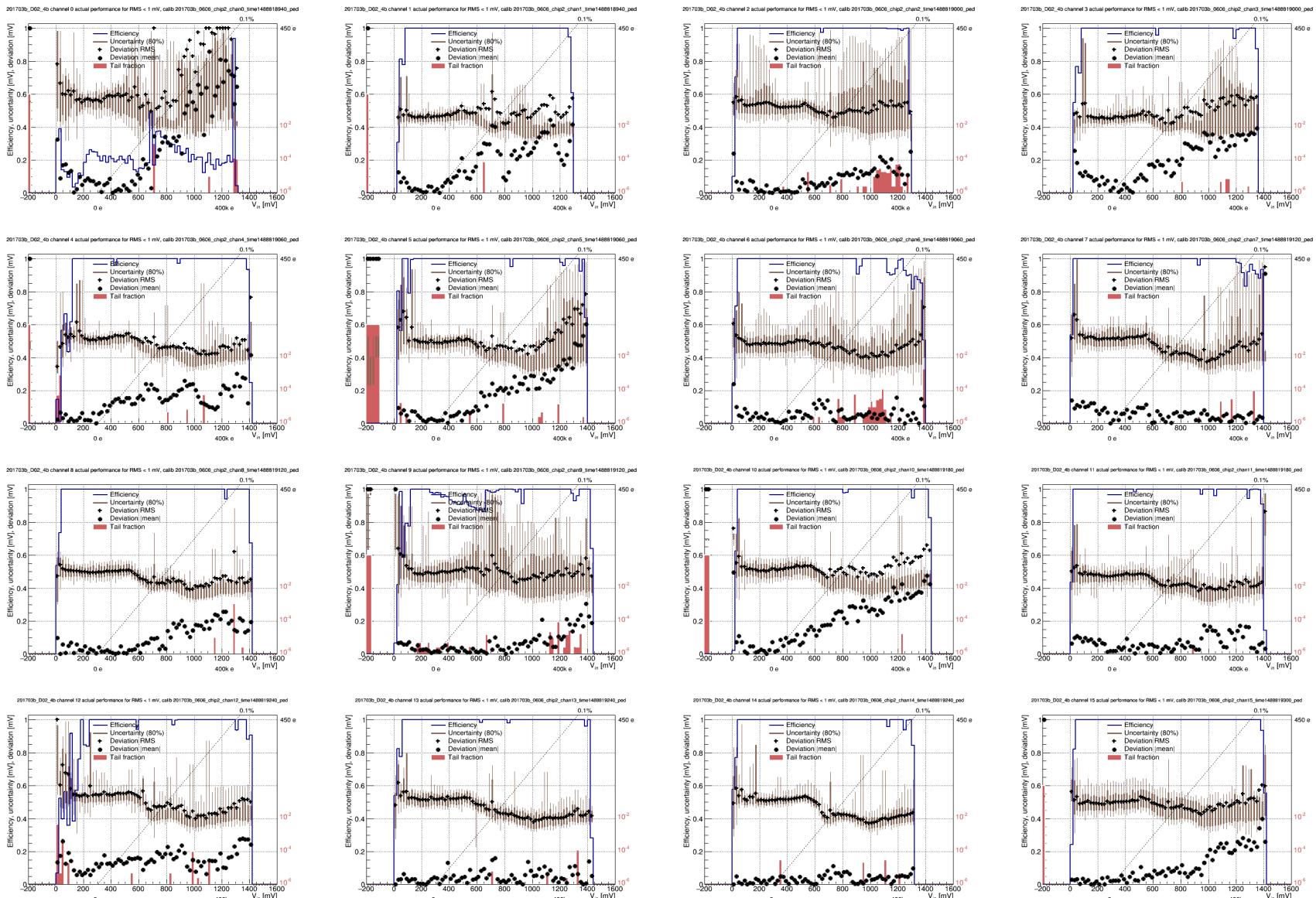
Calibrated performance: chip D02, time 3b



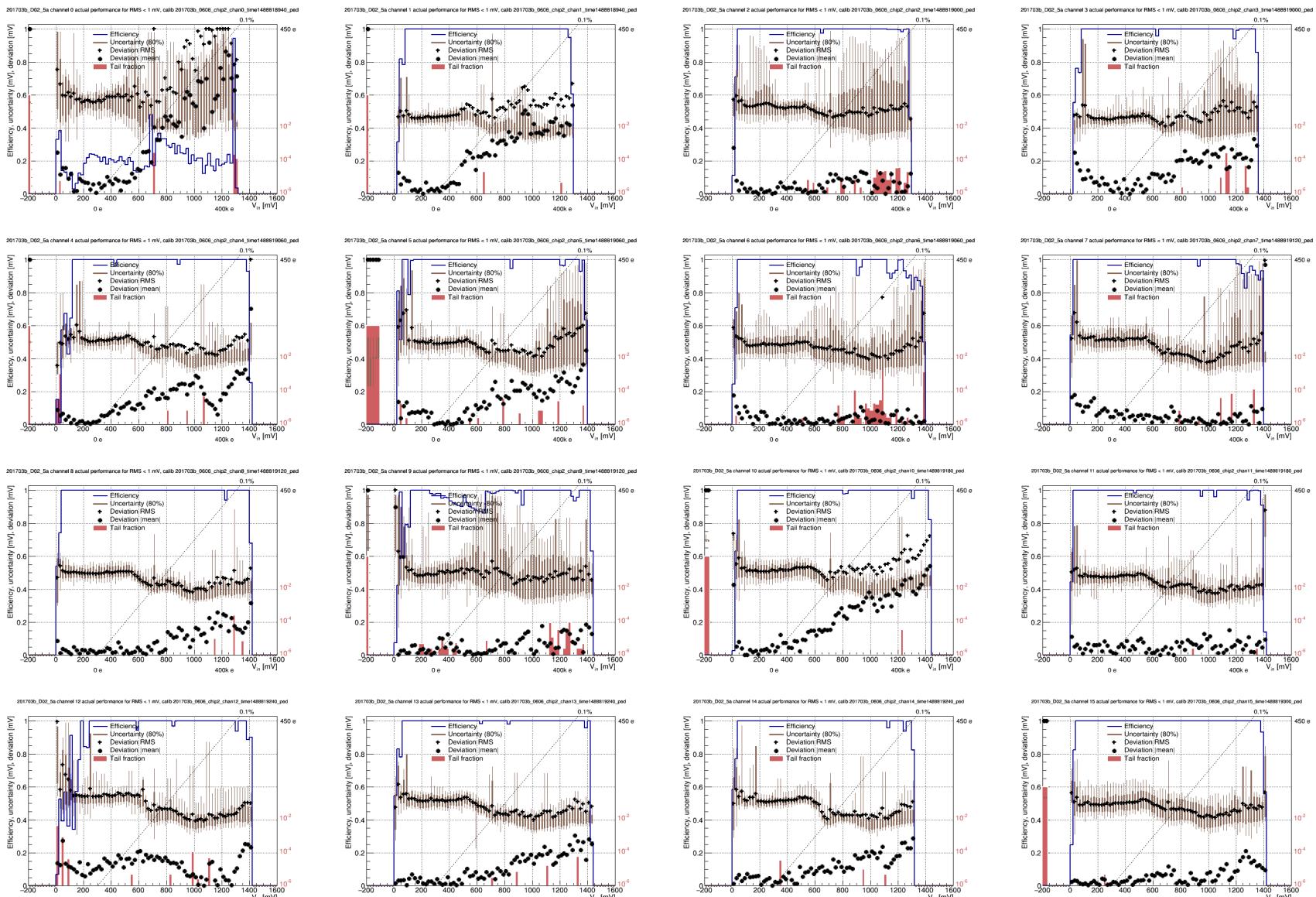
Calibrated performance: chip D02, time 4a



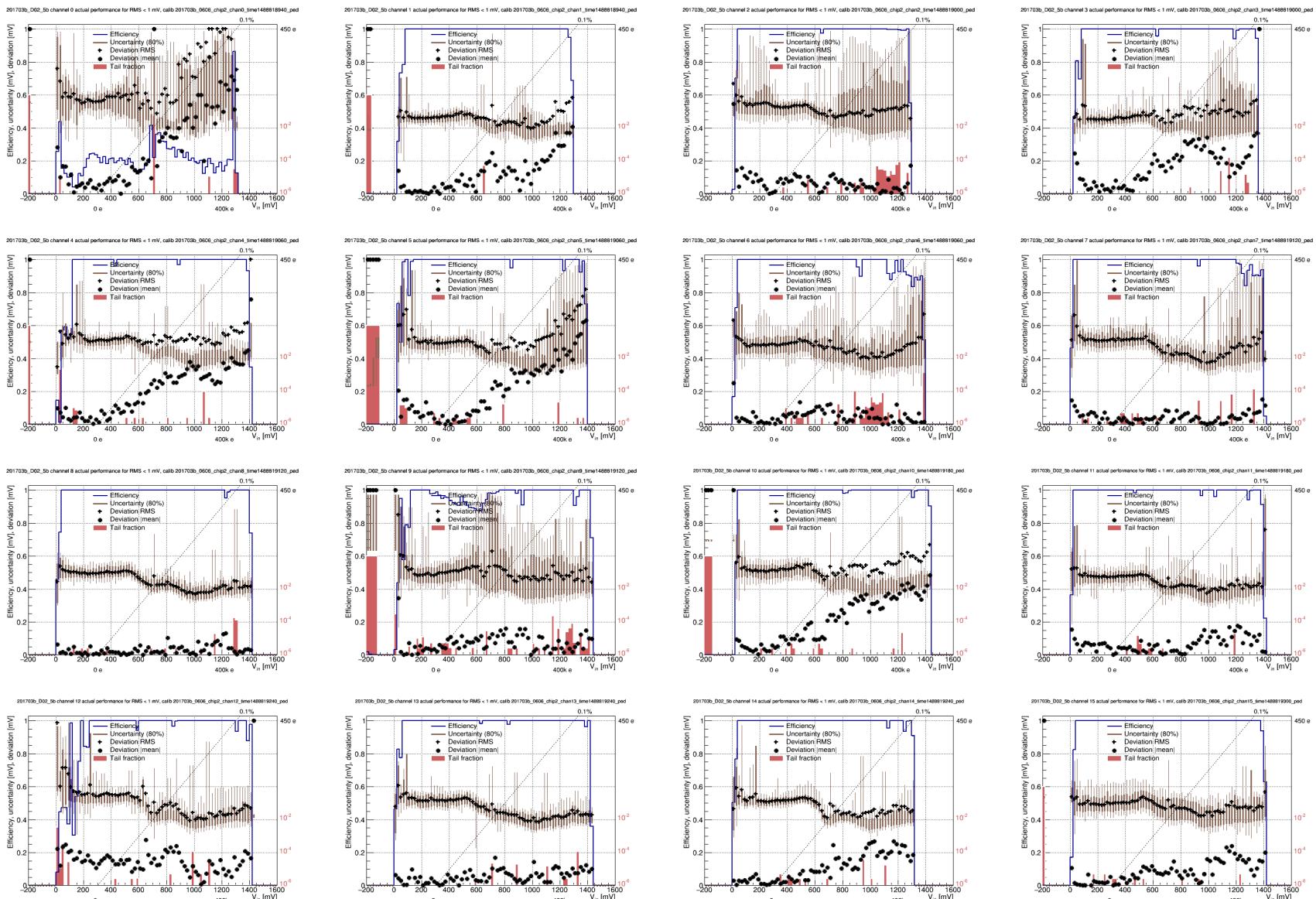
Calibrated performance: chip D02, time 4b



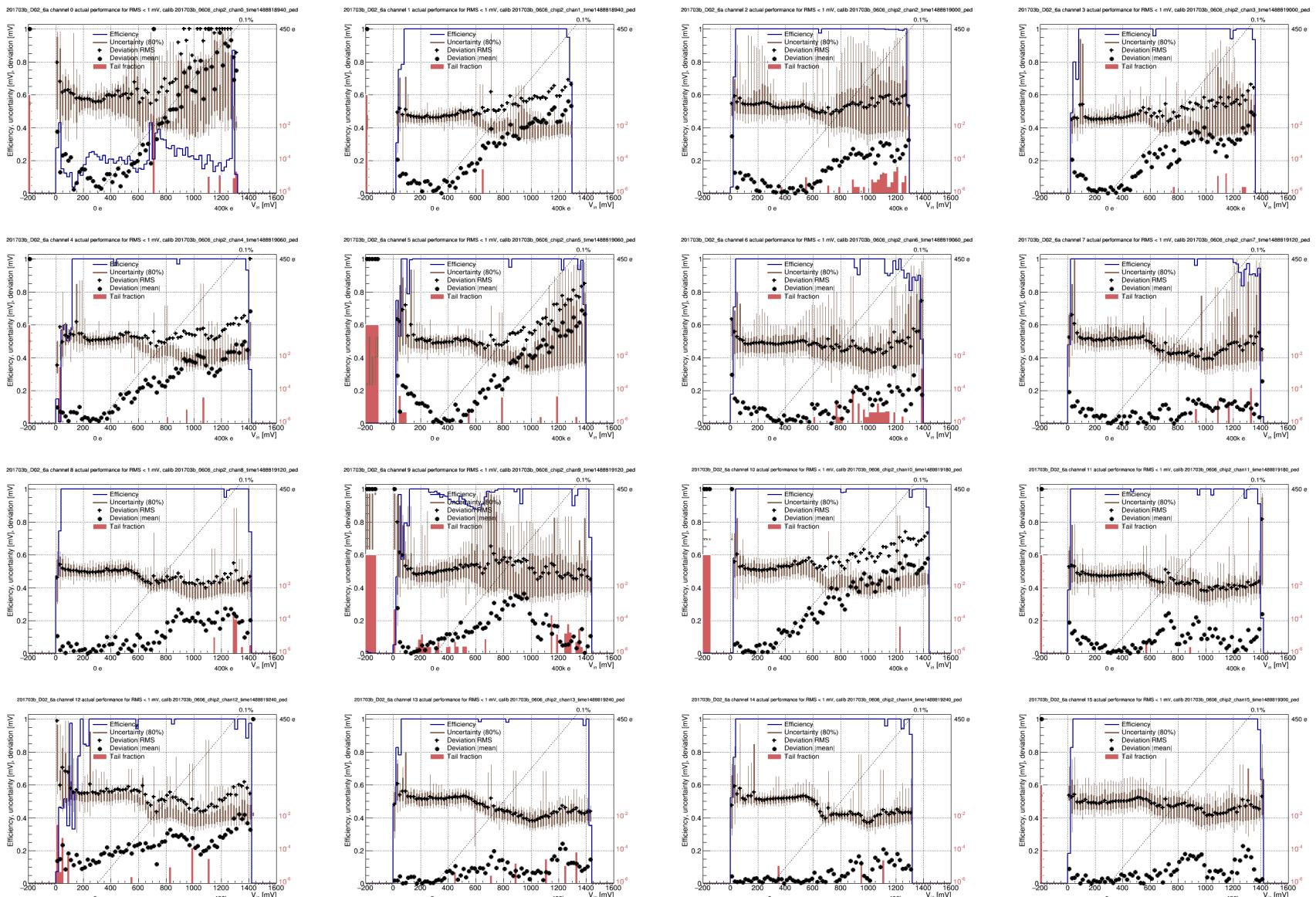
Calibrated performance: chip D02, time 5a



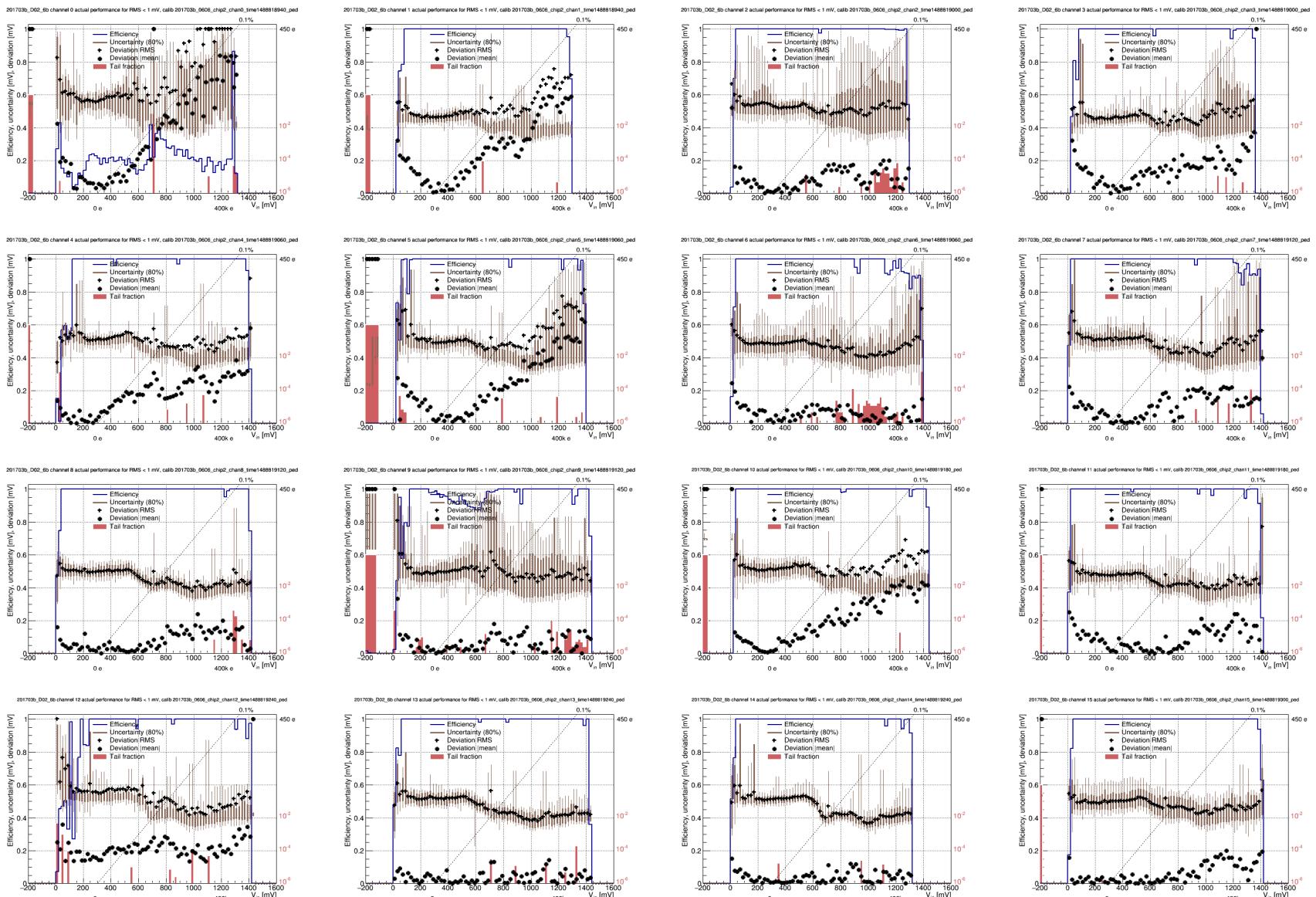
Calibrated performance: chip D02, time 5b



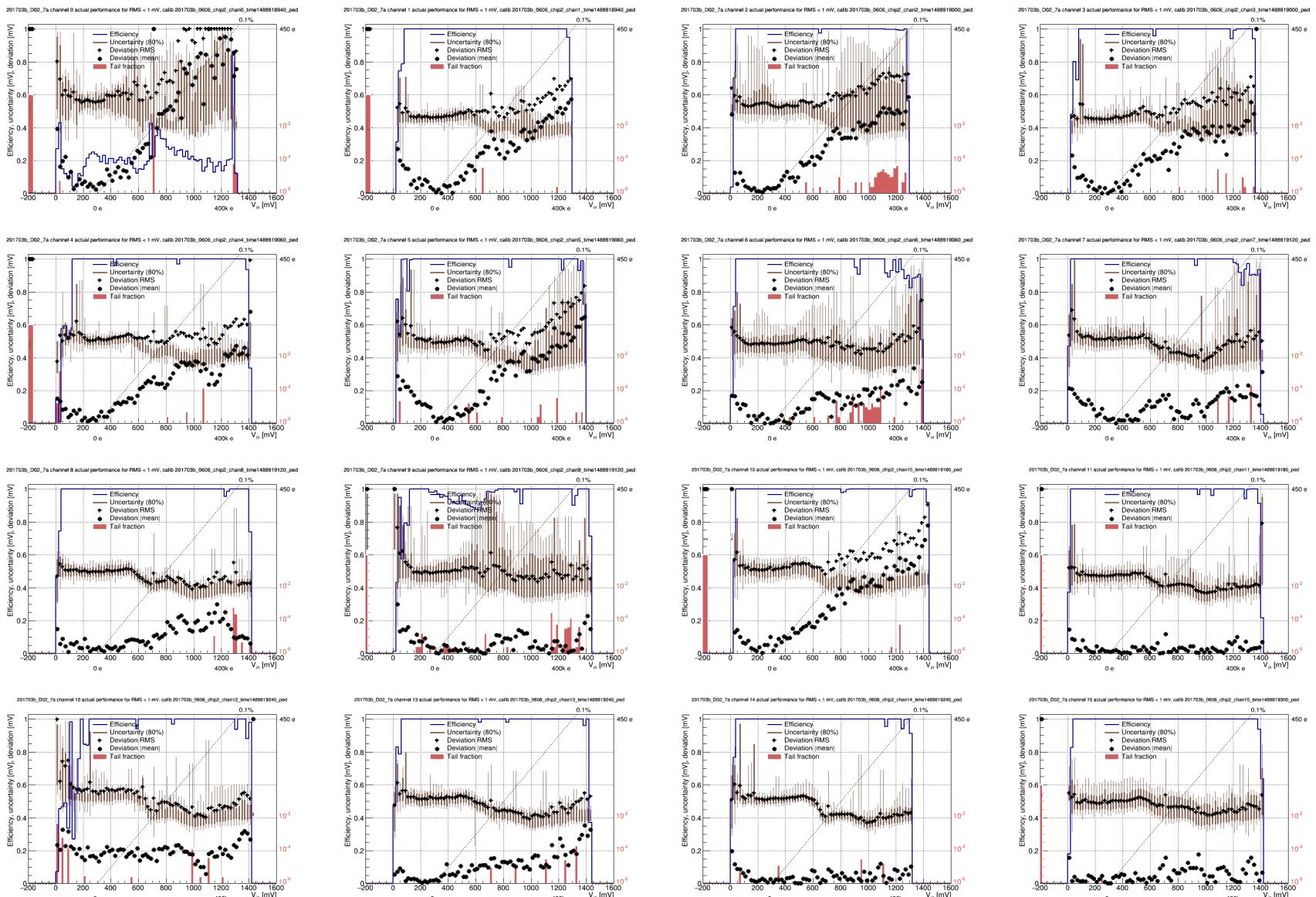
Calibrated performance: chip D02, time 6a



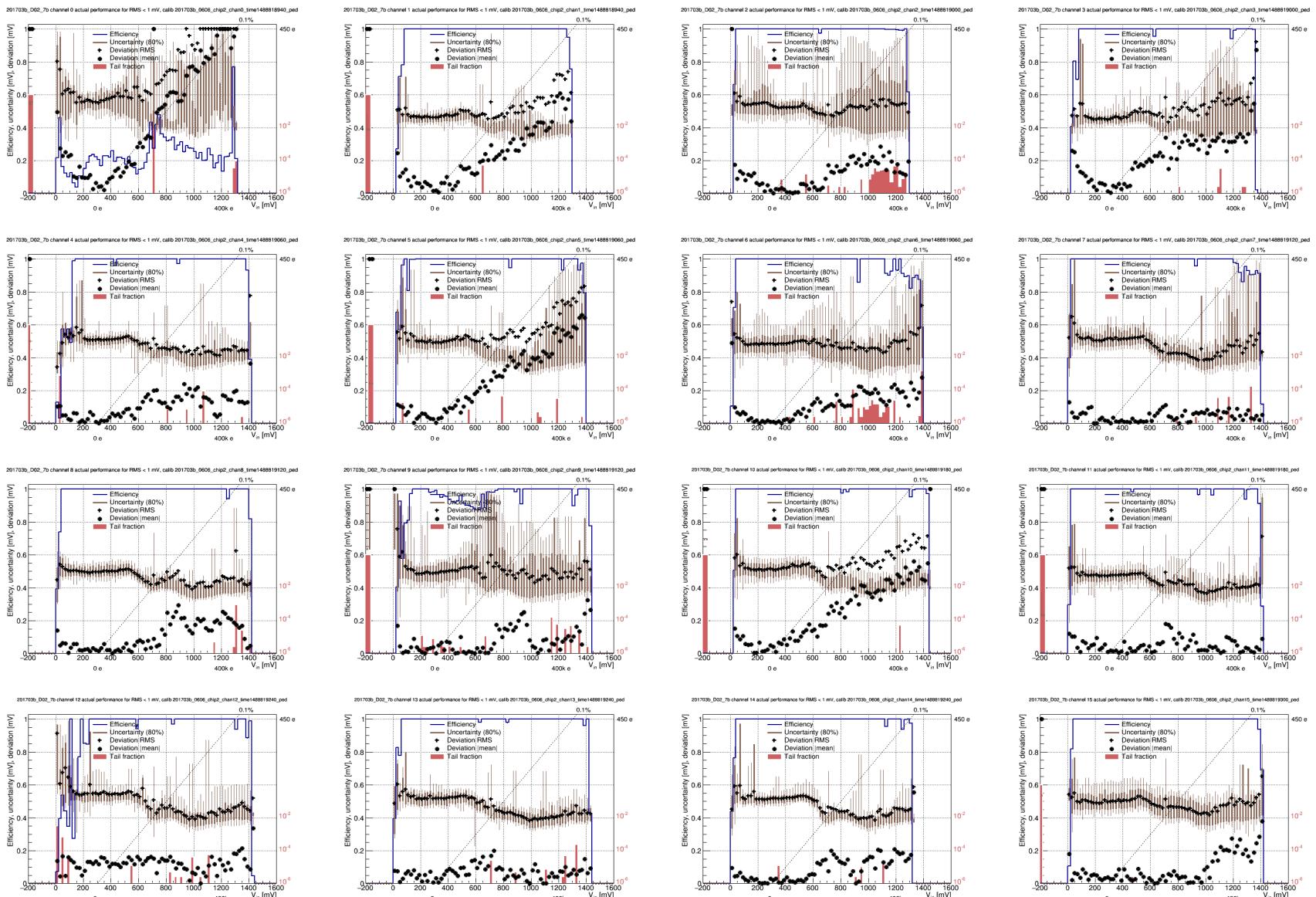
Calibrated performance: chip D02, time 6b



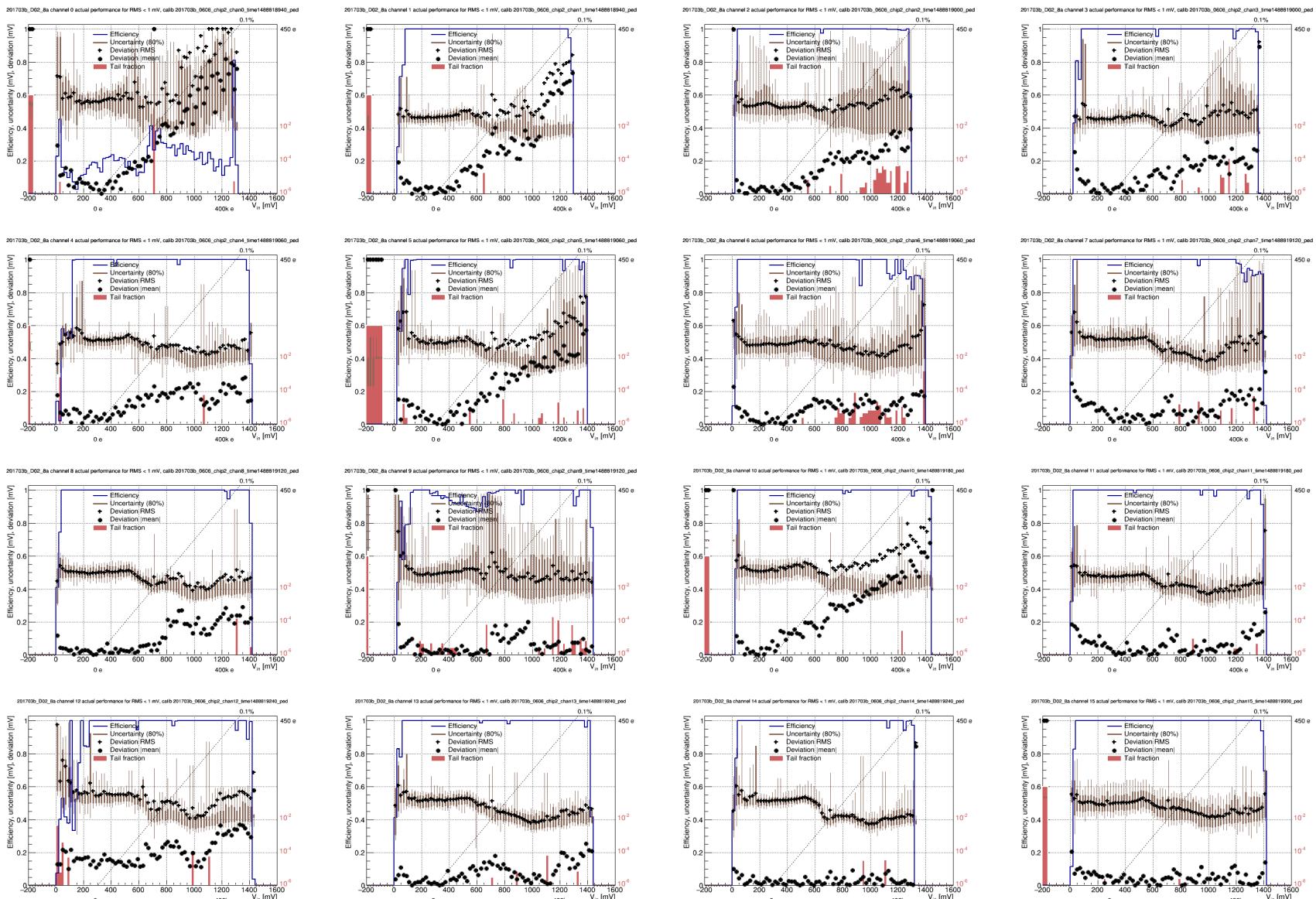
Calibrated performance: chip D02, time 7a



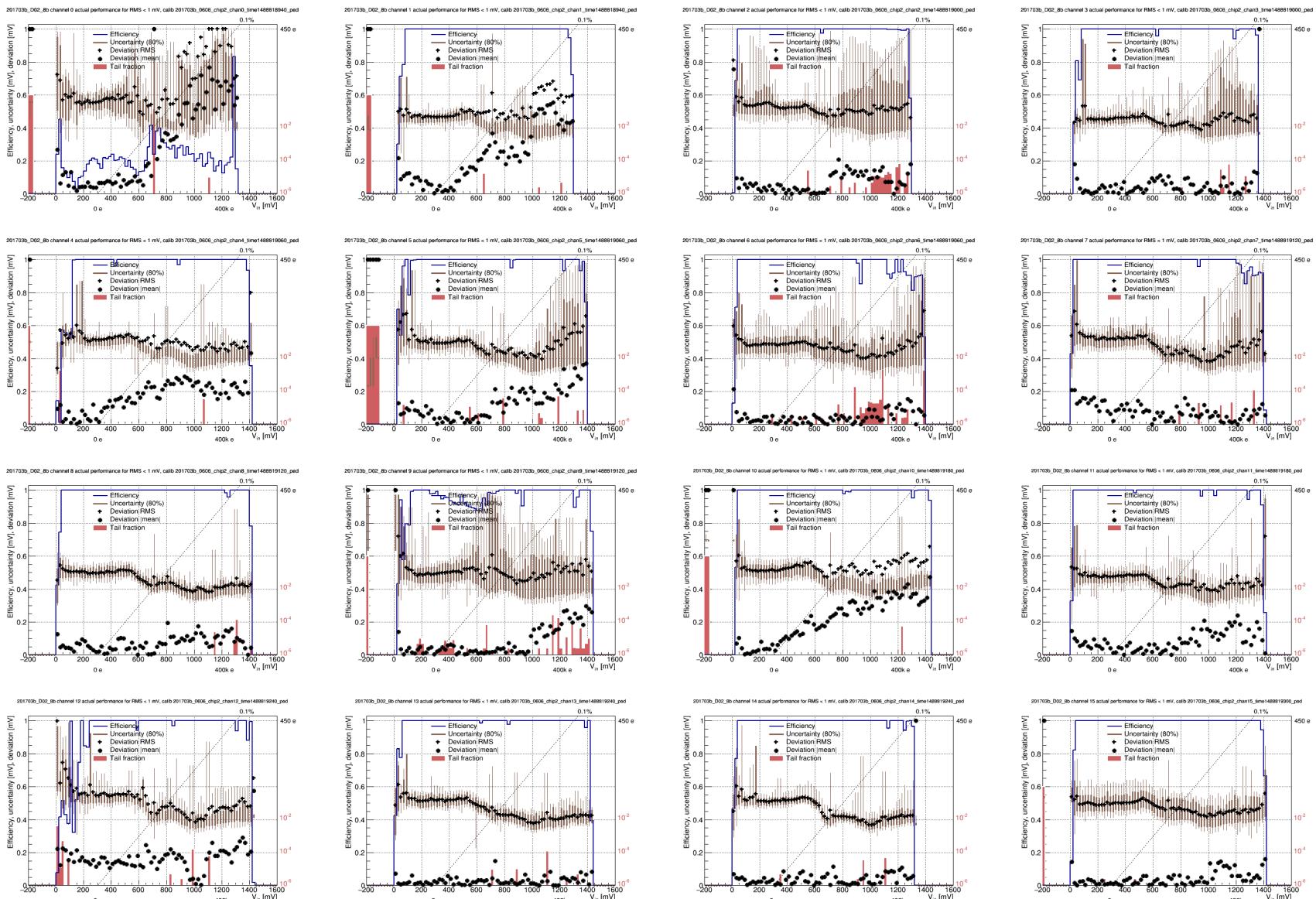
Calibrated performance: chip D02, time 7b



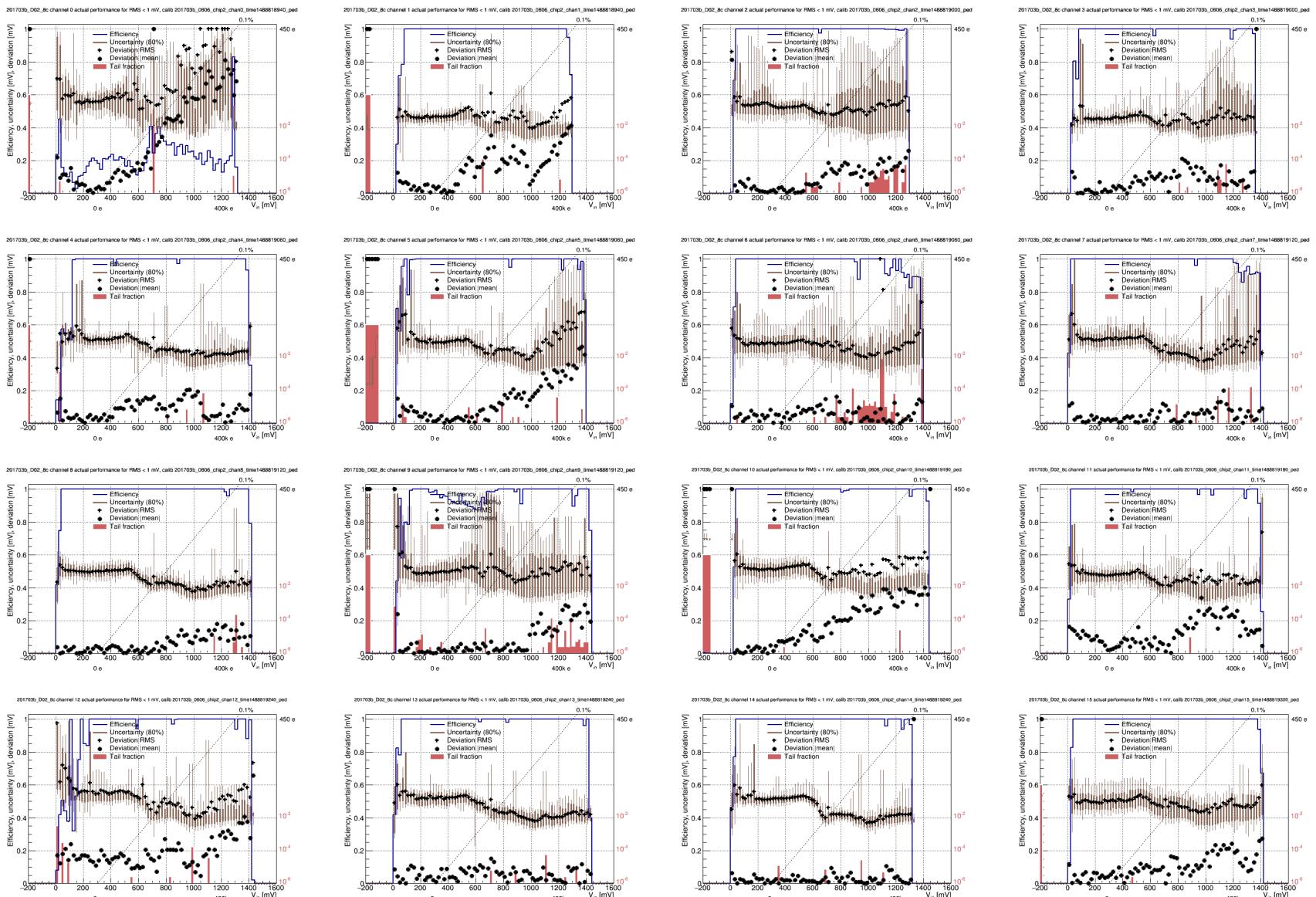
Calibrated performance: chip D02, time 8a



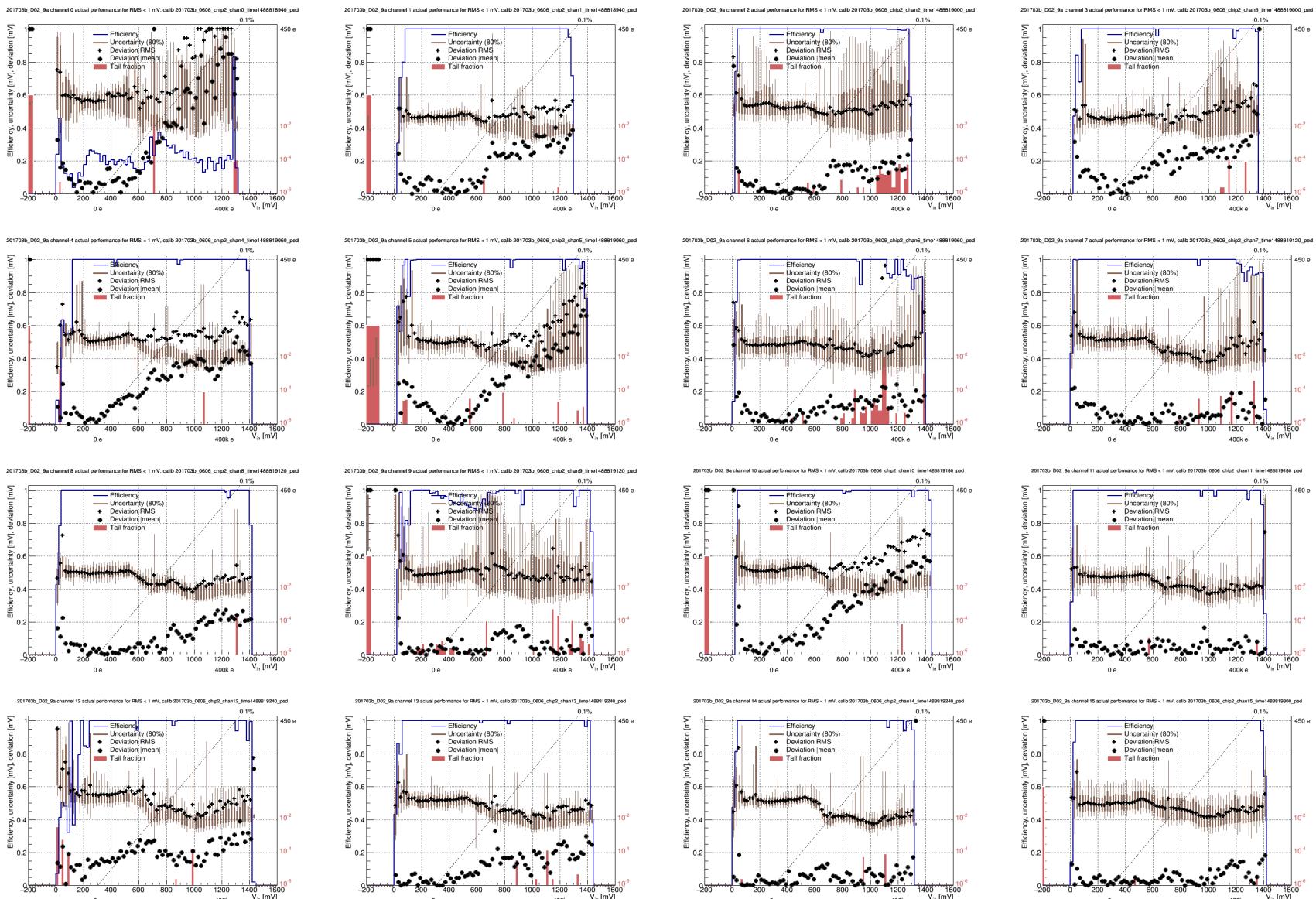
Calibrated performance: chip D02, time 8b



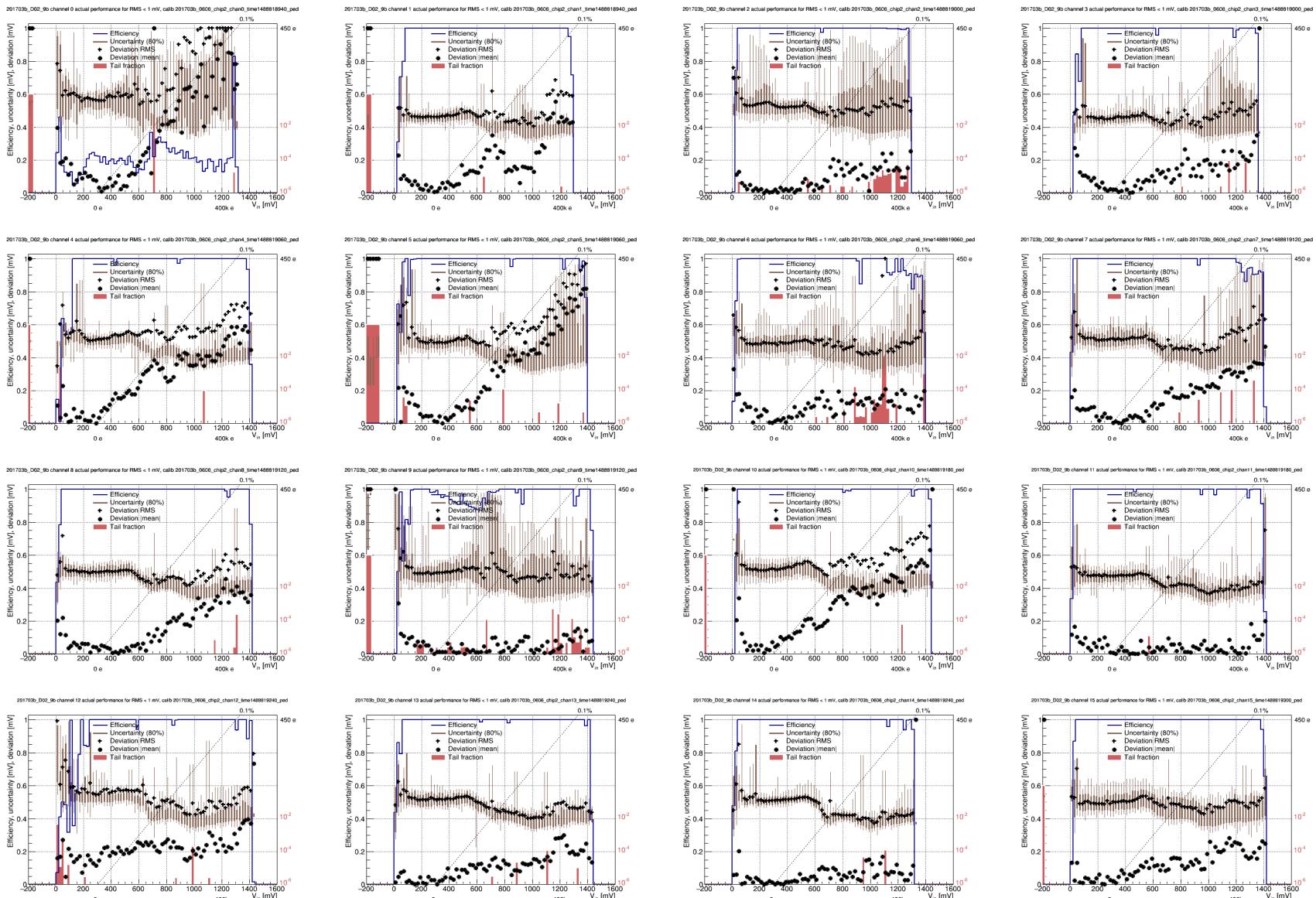
Calibrated performance: chip D02, time 8c



Calibrated performance: chip D02, time 9a



Calibrated performance: chip D02, time 9b



Calibrated performance: chip D02, time 9c

